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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,612	02/19/2004	Joel F. Adam	6259P006	5142
8791 7590 07/06/2009 BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040				
EXAMINER				
FRANKLIN, RICHARD B				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/782,612

**Applicant(s)**

ADAM ET AL.

**Examiner**

RICHARD FRANKLIN

**Art Unit**

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 April 2009.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6, 8-16, 19 and 20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 3-6, 8, 9, 16, 19 and 20 is/are allowed.  
6) ☒ Claim(s) 1, 2 and 10 is/are rejected.  
7) ☒ Claim(s) 11-15 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on 19 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Claims 1 – 6, 8 – 16, and 19 – 20 are pending.

### *Response to Arguments*

2. Applicant's arguments filed 20 April 2009 have been fully considered but they are not persuasive.

As per claim 1, Applicant argues that the relied upon reference, US Patent No. 6,965,336 (hereinafter Osborne), does not teach that the first and second isolator are different from each other, as required by the claim (Response filed 20 April 2009; Page 9). However, the Examiner respectfully disagrees. Osborne states:

Isolation barrier 16 may be a **conventional bi-directional isolation barrier that is implemented using conventional components**, including transformers, capacitors, or **opto-isolators** (emphasis added) (Osborne; Col 4 Lines 17 – 20).

The Examiner submits that while Osborne may not *explicitly* state that isolation barrier 16 includes a plurality of isolators, one for each direction of communications, such a configuration is *inherent* to the system of Osborne. A conventional opto-isolator is unidirectional in nature, meaning it only allows communication in a single direction. Therefore, in order to implement electrical isolation in a bi-directional communication system, a plurality of opto-isolators *must* be used, one for each direction of communications. US Patent 6,408,034 (hereinafter Krone) shows that in order to implement bi-directional communication using opto-isolators, a plurality of opto-isolators are *required* (Krone; Col 4 Lines 15 – 36). In addition to Krone, US Patent No.

5,896,415 (hereinafter Owens) shows that a bidirectional isolator using opto-isolators requires one opto-isolator for each direction of data transfer (Owens; Figure 4, Col 6 Lines 17 – 30).

Please note, US Patent Nos. 6,408,034 and 5,896,415 are relied upon strictly as extrinsic evidence demonstrating the inherency described above and are not intended to be or suggest a rejection under 35 USC 103(a).

Applicant also argues that Osborne does not teach that the first component transfers information via the first isolator *while* the second component transfers information via the second isolator (Response filed 20 April 2009; Page 10). However, it is noted that the above feature is not recited in pending claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Accordingly, Osborne both explicitly and inherently teaches all the limitations of claim 1.

As per claim 10, Applicant argues that Osborne does not teach that the first isolator receives a serial data bit preceded by control information from the first programmable component (Response filed 20 April 2009; Page 10). However, the Examiner respectfully disagrees. Osborne teaches that the first programmable component (Osborne; Figure 2 Item 18) includes communications interface circuitry (Osborne; Figure 2 Item 24) which combines data bits (Osborne; Figure 3 Item 36

"SD<sub>DP</sub>") and clock information (Osborne; Figure 3 Item 38 "SCK<sub>DP</sub>") into a multiplex signal (Osborne; Figure 40 "MX<sub>DP</sub>"). The multiplex signal is then transferred across the isolation barrier (Osborne; Figure 2 Item 16) to the second programmable component (Osborne; Figure 2 Item 28). Therefore the first isolator (Osborne; Figure 2 [isolator in Isolation Barrier 16 for transfer from Item 18 to Item 20, see comments pertaining to claim 1 above]) receives serial data bits SD<sub>DP</sub> combined with control information SCK<sub>DP</sub> from the first programmable component. The second data bit of SD<sub>DP</sub> would be preceded by the clock cycle SCK<sub>DP</sub> of the first data bit, and therefore the serial data bit is preceded by control information.

Applicant also argues that Osborne does not teach a plurality of serial port connectors, as required by claim 10 (Response filed 20 April 2009; Page 11). However, the Examiner respectfully disagrees. Osborne teaches that bi-directional isolation system 10 is connected to both data pump 12 and telephone line 14 (Osborne; Figure 1, Col 4 Lines 21 – 25). Therefore, the interfaces provided for both data pump 12 and telephone line 14 constitute the plurality of serial port connectors of claim 10.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 2 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,965,366 (hereinafter Osborne).

As per claim 1, Osborne teaches a serial line circuit comprising a bus (Figure 2 [Connection between Items 18 and 20]); a plurality of isolators interposed between two portions of the bus (Figure 2 Item 16, Col 4 Lines 17 – 20); a first component coupled to the bus, the first component to transfer information via a first isolator of the plurality of isolators (Figure 2 Item 18); and a second component coupled to the bus, the second component to transfer sampled information over the bus via a second isolator of the plurality of isolators (Figure 2 Item 20). Osborne inherently teaches that the second isolator is different from the first isolator (Osborne; Col 4 Lines 17 – 20, see “Response to Arguments” presented above).

As per claim 2, Osborne also teaches wherein the plurality of isolators is a pair of isolators including the first isolator and the second isolator (Col 4 Lines 1 – 20, see “Response to Arguments” presented above).

As per claim 10, Osborne teaches an electronic device comprising a plurality of serial port connectors (Figure 1 Items 14 and 12, see “Response to Arguments” presented above); and a serial line circuit coupled to the plurality of serial port connectors (Figure 1 Item 10), the serial line circuit comprises a first programmable component (Figure 2 Item 18), a second programmable component in communication

with the plurality of serial port connectors (Figure 2 Item 20), a bus coupled to the first programmable component and the second programmable component (Figure 2 [Connection between Items 18 and 20]), a first isolator situated along the bus (Figure 2 Item 16), the first isolator to receive a serial data bit preceded by control information from the first programmable component for transfer to the second programmable component (Col 4 Lines 56 – 67, see “Response to Arguments” presented above), and a second isolator situated along the bus (Figure 2 Item 16), the second isolator to receive a sampled data bit preceded by control information from the second programmable component for transfer to the first programmable component (Figure 5 Item SD<sub>LS</sub> and Item 62, see “Response to Arguments” presented above).

#### ***Allowable Subject Matter***

4. Claims 11 – 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the first component is a programmable component being a field programmable gate array (FPGA) to multiplex serial data received from a plurality of serial Universal Asynchronous Receiver Transmitters (UARTs) and to transfer the serial data over the bus via the first isolator***, as required by dependent claim 11, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches multiplexing serial data

with overhead data (Osborne; Col 4 Lines 56 – 67) by communications interface circuitry and transferring serial data by the first isolator, but does not teach wherein the first component is an FPGA and the serial data is received from a plurality of UARTs.

Claim 12 is also objected to as depending from claim 11 which is objected to as allowable above.

Claim 13 would be allowable because the prior art of record fails to teach or suggest alone or in combination ***wherein the first programmable component of the serial line circuit to receive serial data bits including the serial data bit, to multiplex the received serial data bits by forming data frames, one of the data frames including a serial port number along with the serial data bit, and to transfer the serial port number along with the serial data bit to the second programmable component over the bus via the first isolator***, as required by dependent claim 13, ***in combination with the other recited claim limitations*** (emphasis added). The prior art of record teaches multiplexing data bits with control information (Osborne; Col 4 Lines 56 – 67), but does not teach including a serial port number along with the serial bit and transferring the serial port number along with the serial bit to the second component over the bus via the first isolator.

Claims 14 and 15 are also objected to as depending from claim 13 which is objected to as allowable above.

5. Claims 3 – 6, 8 – 9, 16 and 19 – 20 are allowed.



6. The following is an examiner's statement of reasons for allowance:

Claim 3 is allowed because the prior art of record fails to teach or suggest alone or in combination **wherein the first component is a programmable component being a field programmable gate array (FPGA) to multiplex serial data and to transfer the serial data over the bus via the first isolator**, as required by dependent claim 3, **in combination with the other recited claim limitations** (emphasis added). The prior art of record teaches multiplexing serial data with overhead data (Osborne; Col 4 Lines 56 – 67) by communications interface circuitry and transferring serial data by the first isolator, but does not teach wherein the first component is an FPGA multiplexing serial data.

Claim 4 is also allowed because of its dependency upon allowed independent claim 3.

Claims 5 – 6 and 8 – 9 are allowed because Applicant has amended claim 5 to be independent and include subject matter which was indicated as allowable in the previous office action (See office action mailed 04 February 2009; indication of allowable subject matter in claim 7).

Claims 6 and 8 – 9 are allowed because of their dependency upon allowed independent claim 5.

Claims 16 and 19 – 20 are allowed because Applicant has amended claim 16 to include subject matter which was indicated as allowable in the previous office action

(See office action mailed 04 February 2009; indication of allowable subject matter in claim 18).

Claims 19 – 20 are allowed because of their dependency upon allowed independent claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. US Patent No 6,408,034: Demonstrates the inherent teachings of Osborne as shown above.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD FRANKLIN whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2181

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